

PREPARED BY: <i>K. Inoue K. Miki</i> DATE: 5. APR. 1996	<h1>SHARP</h1> <p>ELECTRONIC COMPONENTS GROUP SHARP CORPORATION</p> <h2>SPECIFICATION</h2>	SPEC NO. EC-96413 -
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APPROVED BY: <i>K. Ishii</i> DATE: 5. APR. 1996		ISSUE 5. APR. 1996 PAGE 8 REPRESENTATIVE DIVISION <input checked="" type="checkbox"/> ELECTRONIC COMPONENTS DIV. <input type="checkbox"/> OPTICAL DEVICE DIV. <input type="checkbox"/> PILOTO VOLTAICS DIV.

DEVICE SPECIFICATION FOR
 DBS TUNER WITH FM DEMODULATOR

MODEL NO. **BSFH78G52**

CUSTOMER'S APPROVAL

DATE _____

BY _____

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Description: This specification covers DBS Tuner with FM demodulator intended for use in Satellite Receiver

1. GENERAL SPECIFICATIONS

1-1 Receiving frequency range		900 MHz to 2150 MHz
1-2 Input level		-60dBm ~ -30dBm
1-3 Nominal input impedance		75 ohm
1-4 Intermediate frequency		479.5 MHz
1-5 Channel selection system		Frequency Synthesizer with 1 ² C bus "SP5655S or SP5055DS,GS or TSA5055T/C2,C3" (clock 4.0MHz)
1-6 Operating voltage	(B2)	5.0V ± 0.3V
ODU Power	(E1)	25V, 400mA max.
Tuning voltage	(TUN)	30.0V ± 1.5V DC
1-7 IF Band width		27MHz (3dB down) typ. 18MHz (3dB down) typ.
1-8 Demodulation system		PLL
1-9 Input structure		F type (Female)
1-10 Circuit block diagram		Figure 1
1-11 Connection diagram		Figure 3
1-12 Video Circuit for measurement		Figure 4

2. MECHANICAL SPECIFICATION

2-1 Dimension and mounting details		Figure 2
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3. ENVIRONMENTAL SPECIFICATIONS

3-1 Temperature		
Operating		0℃ to 50℃
Storage		-20℃ to 70℃
3-2 Humidity		
Operating		Less than 85%
Storage		Less than 90%

4. TESTING CONDITION

4-1 Supply voltage	(B2)	5.0V ± 0. V
	(TUN)	30.0V ± 0.1V
4-2 Ambient temperature		25℃ ± 5℃
4-3 Ambient humidity		65% ± 10%
4-4 Test signal (PAL)		
Modulation System:		FM, positive
Pre-Emphasis Characteristic:		CCIR Report 405-1(B)
Video deviation:		16MHzpp

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ELECTRICAL SPECIFICATIONS

(Testing Condition is showed 4-1-4-4)

No.	Item	Specification			Unit	Condition
		Min	Typ	Max		
6-1	Noise figure		8	15	dB	
6-2	Image rejection	30	40		dB	
6-3	Input VSWR		2	3		
6-4	Drift of local oscillation frequency		±10		MHz	25°C ± 25°C
6-5	Intermodulation rejection	40	60		dB	Input level -35dBm Desired signal Fo Undesired signal (2 signals) (Fo+29.5MHz, Fo+59MHz) (Fo-29.5MHz, Fo-59MHz)
6-6	Local oscillation signal leak at input terminal			-63	dBm	900~1750MHz
				-50	dBm	1750~2629.5MHz
6-7	Output level	0.55	0.7	0.9	Vpp	1MΩ load deviation 16MHzpp *1
6-8	Frequency response (Mag)			±2	dB	50Hz~8.4MHz
				±3	dB	8.4MHz-10.5MHz
						(reference: 100KHz) *1
6-9	DG		2	7	%pp	Video circuit for measurement is connected APL=50% *1,2
6-10	DP		2	5	%pp	
6-11	SN(C/N=14dB)	35			dB	Video circuit for measurement is connected *1
6-12	Static threshold		6	8	dB	100HZ-5.0MHZ *1 FM deviation 16MHzpp
6-13	Current consumption			4	mA	TUN
			220	330	mA	B2
6-14	AFT Dead zone		400		KHz	*(Refer to 6-4.)
6-15	AFT Preset error	-1		+1	MHz	Ta=25°C

*1 Refer figure 3

*2 BW=27MHz



[61 PLL FUNCTIONAL DESCRIPTION
6-1.I²C-BUS DATA FORMATS

	MSB					LSB				
ADDRESS	1	1	0	0	0	MA1	MA0	o	A	BYTE 1
PROGRAMMABLE DIVIDER	o	N ₁₄	N ₁₃	N ₁₂	N ₁₁	N ₁₀	N ₉	N ₈	A	BYTE 2
PROGRAMMABLE DIVIDER	N ₇	N ₆	N ₅	N ₄	N ₃	N ₂	N ₁	N ₀	A	BYTE 3
CHARGE PUMP AND TEST BITS	1	0	0	0	1	1	1	0	A	BYTE 4
IO PORT CONTROL BITS	0/1 (P7)	0/1 (P6)	o (P5)	o (P4)	o	d	d	0/1 (Po)	A	BYTE 5

Table 1 Write data format(MSB is transmitted first)

ADDRESS	1	1	0	0	0	MA1	MA0	1	A	BYTE 1
STATUS BYTE	POR	FL	12	11	IO	A2	A1	A0	A	BYTE 2

Table 2 Read data format

LSB bit of BYTE 1: Mode selection (0: Write mode, 1: Read mode)

A: Acknowledge Bit

MA1, MA0: Variable address bits(see Table 4).

No-N14: Programmable divider bit data.

PO: Open

P3: Output from tuner

P4: (Digital AFT 1)

P5: (Digital AFT 2)

P6: IF Band width selection (0: BW=18MHz, 1: BW=27MHz)

P7: Output from tuner

POR: Power On Reset indicator

FL: Phase Lock detect Flag

12,11,10: Digital information from Ports P7,P5 and P4, respectively

A2, A1,A0: 5 Level ADC data from P6 (see Table 3)

MA1	MA0	Voltage input to P3
o	0	0 ~ 0.1*B2
o	1	ALWAYS VALID
1	0	0.4*B2 ~ 0.6*B2
1	1	0.9*B2 ~ B2

Table 4 Address selection(B2:5V)

A2	A1	A0	Voltage input to P6
1	0	0	0.6*B2 ~ B2
o	1	1	0.45*B2 ~ 0.6*B2
o	1	0	0.3*B2 ~ 0.45*B2
o	0	1	0.15*B2 ~ 0.3*B2
o	0	0	0 - 0.15*B2

Table 3 ADC levels (B2: 5V)

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6-2. Programmable divider bits data

The programmed frequency (local oscillator frequency: F_{LO}) can be calculated by multiplying the programmed division ratio by 16 times the comparison frequency (7.8125kHz)

$$N = N_{14} \times 2^{14} + N_{13} \times 2^{13} + \dots + N_1 \times 2 + N_0$$

Local oscillator frequency : F_{LO}

$$F_{LO} = 16 \times N \times 7.8125$$

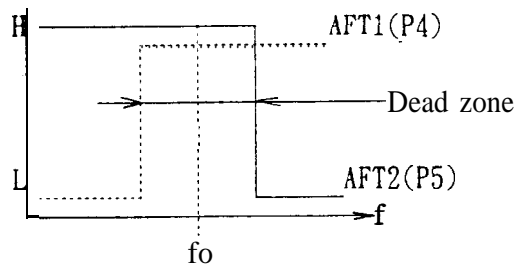
$$= 125 \times N \quad (\text{kHz})$$

(Minimum step size: 125 kHz)

6-3. Input Voltage (SCL, SDA)

Item	MIN	MAX	UNIT
『H』 Level Voltage	3	5.3	V
『L』 Level Voltage	0	1.5	

6-4. AFT CHARACTERISTIC



f: Input frequency
fo: Select frequency

6-5. note

This tuner have I²C bus ports as following table.

Tuner pin No.	I ² C port	note
17	P7	feed thru capacitor 100PF
18	P3	
14	SDA	via series resister 100Q and feed thru capacitor 100PF
16	SCL	

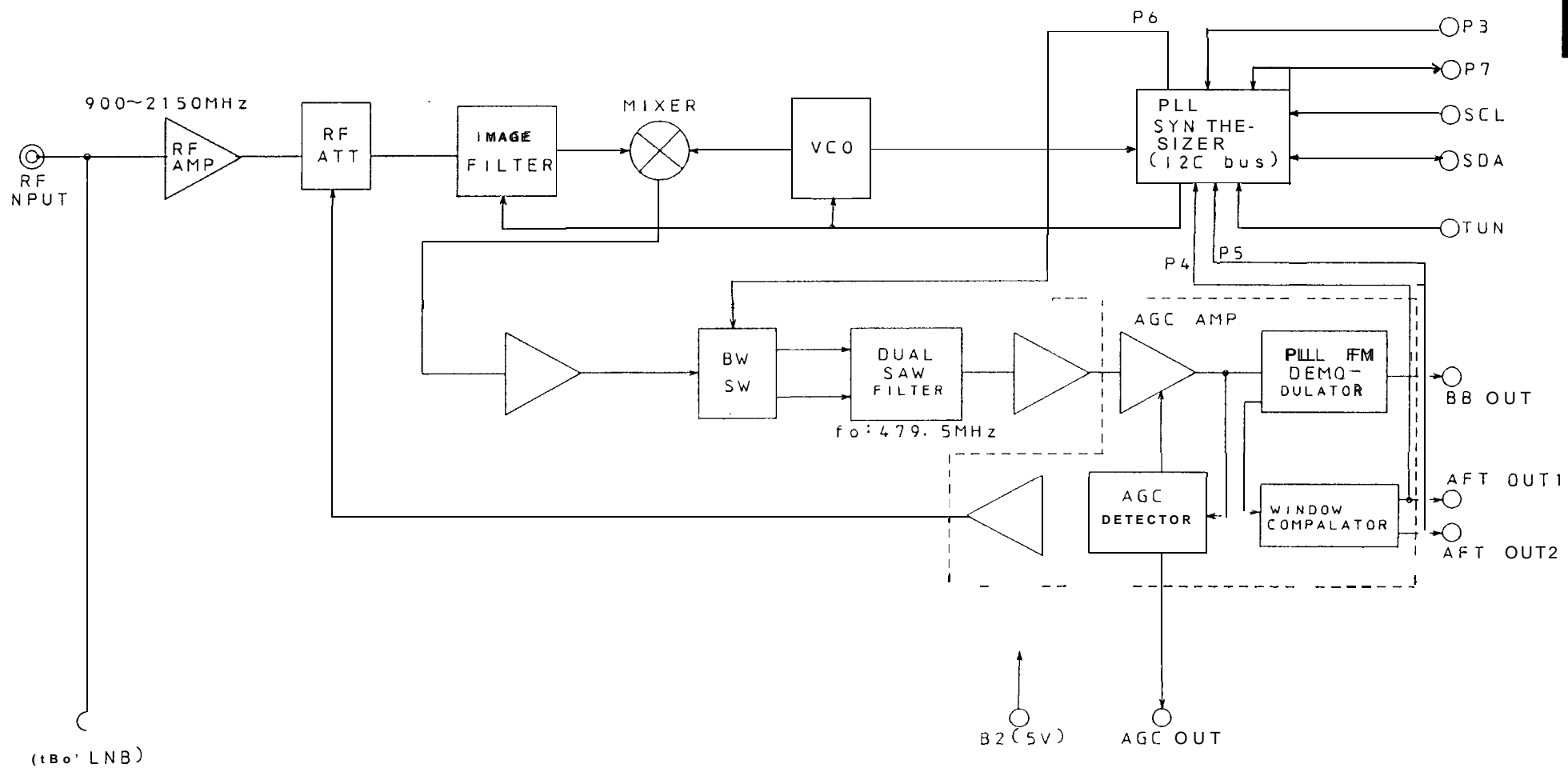


FIGURE 1. CIRCUIT BLOCK DIAGRAM

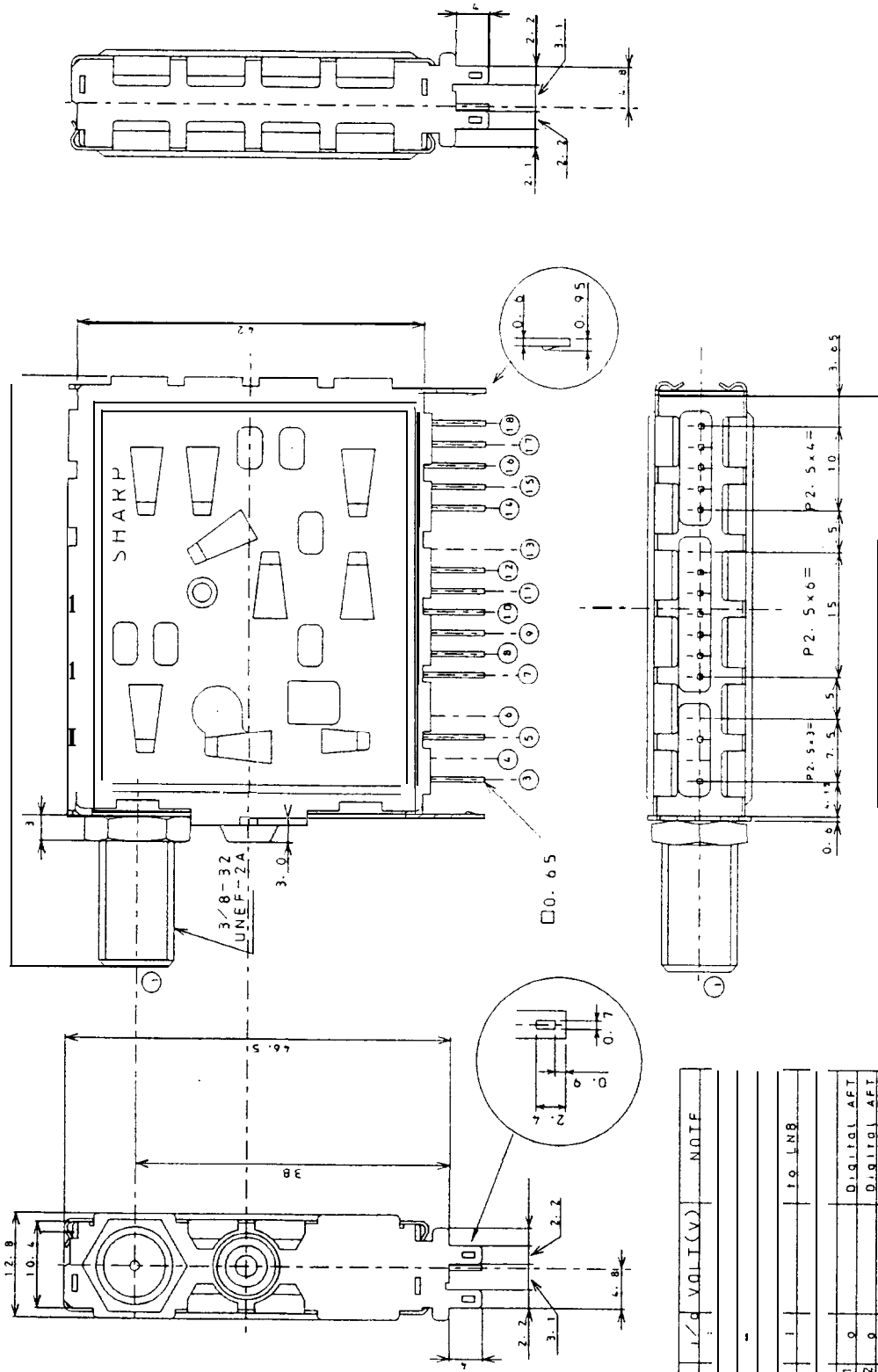


Figure 2 : Dimension and mounting details

NO.	NAME	1/2	VOLTS(V)	NOTE
1	BE IN			
2	NC			
3				
4	B1(LNB)	1		10 LNB
5				
6	AFT OUT1	0		DIGITAL AFT
7	AFT OUT2	0		DIGITAL AFT
8	AGC	0		AGC OUT
9	B2	1	+5V	
10	Base Band	0		BB OUT
11				
12				
13				
14	TUN	1	+30	
15	SCL	1		

SCALE	UNIT (in./mm)	PIECES	MODEL	BSFH7BG52	NAME	OUT LINE DRAWING
FINISH			MATERIAL			
DATE		REVISE				

DATE: 11/11/01
 REVISE: 1
 DRAWN BY: [Signature]
 CHECKED BY: [Signature]
 APPROVED BY: [Signature]
 SHARP CORPORATION

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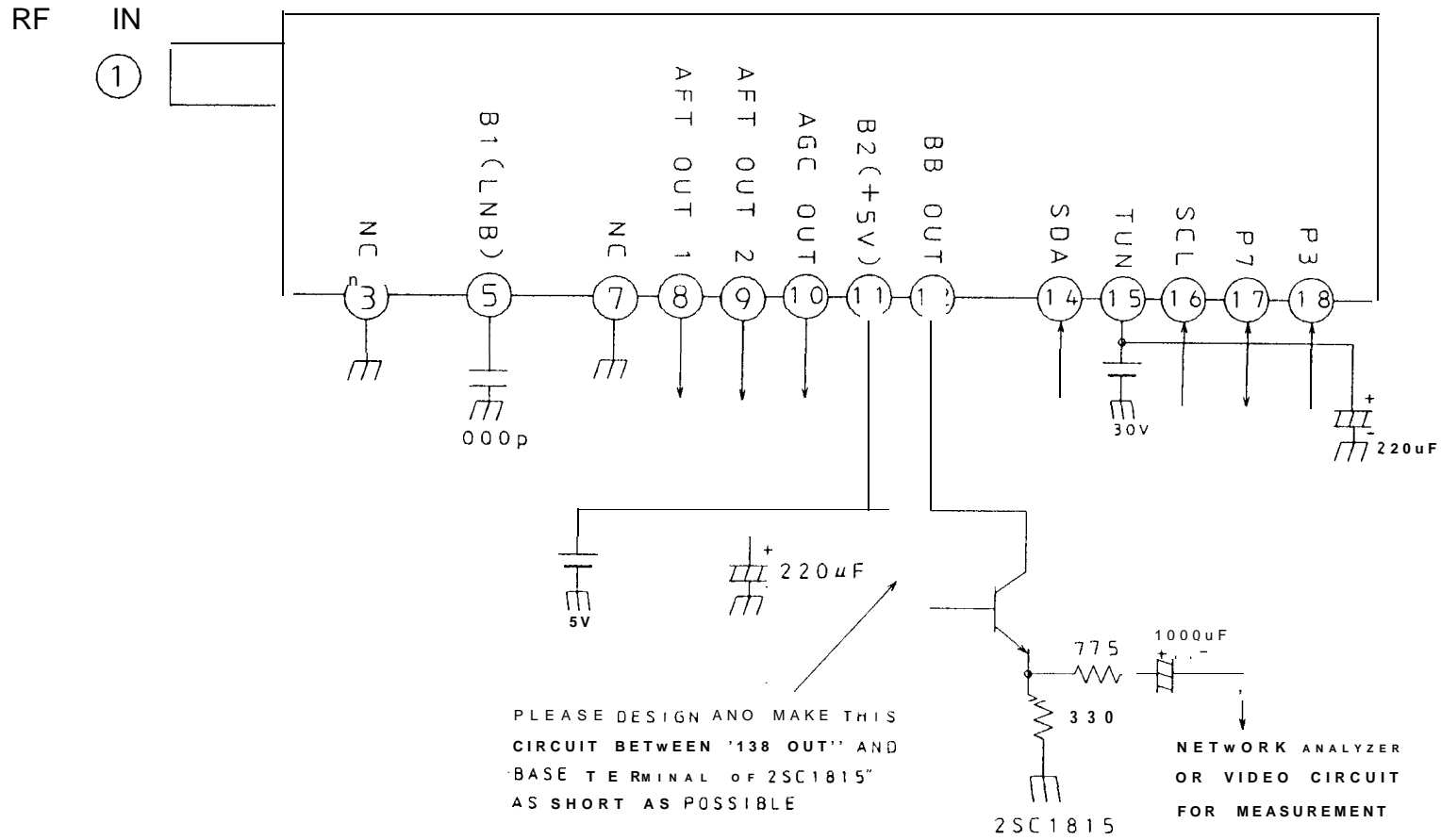


Figure 3. CONNECTION DIAGRAM

